Boosted chemistry at cryogenic temperature for silicon and silicon compound plasma etching

R. Dussart[1], T. Tillocher[1], L. Becerra[1], P. Lefaucheux[1]
[1]*GREMI, Université d'Orléans – CNRS, Orléans, France*

Abstract: Even if it seems counterintuitive, cooling the substrate to very low temperatures can favor chemical reactions and significantly increase the etch rate (ER). Cryogenic etching has been studied for silicon deep etching, but it has also been applied to low-K material etching and Atomic Layer Etching (ALE). More recently, HF-based plasmas with high-energy ion bombardment have been successfully developed to etch SiO_2 and Si_3N_4 at low temperatures. In-situ characterizations of plasma-surface interaction at cryogenic temperature will be presented for different fluorine-based chemistries.

1. Introduction

Cryogenic etching was first introduced in 1988 for silicon etching [1]. The idea was to freeze chemical reactions on the sidewalls of the silicon trenches in an SF_6 plasma to form anisotropic profiles. A few years later, it was shown that a passivation mechanism with oxygen was responsible for protecting the sidewalls from etching. Instead of freezing the chemical reactions, the very low temperature (-120°C) actually favored them at the sidewalls to form a SiO_xF_y layer stable at low temperatures only. The role of SiF_4 molecules, which are the main by-products in silicon etching with SF_6 plasma was highlighted and SiF_4/O_2 plasma was used to reinforce the passivation layer in the so-called STiGer process [2]. Cryogenic etching processes have also been developed for ultra low-K etching without damage [3] and for ALE [4] taking advantage of the enhanced physisorption of certain radicals at low temperature. Recently, HF/H_2O-based plasmas were successfully developed to etch at low temperature thin SiO_2 and Si_3N_4 layers alternatively stacked on silicon for 3D-NAND device applications [5]. Very high aspect ratio holes without defect were obtained showing the very effective effect of the low temperature.

2. Layer stoichiometry tuned with temperature in SiF_4/O_2 plasma

Quasi-in situ XPS characterizations were carried out at IMN (Nantes) on SiO_xF_y layers deposited on silicon in SiF_4/O_2 plasma without bias. The analysis shows a significant change in layer composition when the sample is cooled at -100°C compared to -65°C while operating with the same plasma conditions. This change in the SiO_xF_y composition is very consistent with the mass spectrometry desorption experiments performed during heating of the sample. In particular, the fluorine content of SiO_xF_y was significantly enhanced at -100°C. This passivation layer can be etched by SF_6 plasma. The ER is reduced at low temperatures, but it significantly increases if H_2 is added to the plasma. The role of HF formation at the surface at low temperature can explain this result.

3. HF-based plasmas for dielectric etching

A plasma mixture of HF and H_2O was successfully used to etch 100 nm diameter holes in alternatively deposited SiO_2 and Si_3N_4 layers for 3D NAND device applications [5]. Holes of up to 10 µm deep were obtained with a very vertical side wall. Lowering the temperature to -70°C significantly increased the ER of SiO_2. PF_3 gas additive was also used to further improve the ER. To further study the etch mechanisms, experiments in SF_6/H_2 plasma were carried out in an ICP reactor equipped with a cryogenic chuck. Fig.1 shows the effect of temperature on the ER, which reaches about 1µm.min^{-1} at -150°C. It should be noted that a high bias power (150 W on 4" wafers) was used for this experiment. It is clear from this result that chemistry at the surface is promoted by cooling the substrate.

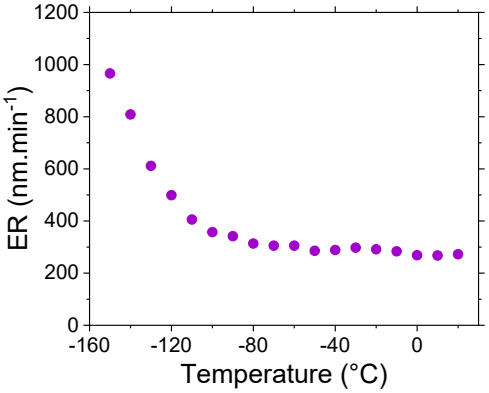

Fig. 1. Etch rate of SiO_2 in SF_6/H_2 inductively coupled plasma versus temperature

Acknowledgement
The authors would like to acknowledge ANR (ANR-20-CE24-0014 project)

References

[1] S. Tachi, K. Tsujimoto, and S. Okudaira, Appl. Phys. Lett. **52** (8) 616 (1988).
[2] R. Dussart et al., J. Phys. D: Appl. Phys. **47** 123001 (2014)
[3] F. Leroy et al., J. Phys. D: Appl. Phys. **48**, 435202 (2015)
[4] G. Antoun et al., Scientific Reports, 11, 357 (2021)
[5] Y. Kihara et al., IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 1-2 (2023).